THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAO TAGUCHI
and TSUYOSHI HIGUCHI

Appeal No. 97-1694
Application 08/351,064[1]

ON BRIEF

Before KRASS, MARTIN, and BARRETT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

[1] Application for patent filed November 28, 1994, entitled (as amended) "Termination Circuits And Related Output Buffers," which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application 5-297669, filed November 29, 1993, Japanese Application 6-030470, filed February 28, 1994, and Japanese Application 6-030501, filed February 28, 1994.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 40, 41, 43, and 55.

We affirm-in-part.

BACKGROUND

The invention is directed to a termination device for a bus in which negligible current flows through the termination device when no signal is transmitted via the bus.

Claim 40 is reproduced below.

> 40. An electronic system comprising:
>
> a plurality of electronic circuits having a signal input and output function and a push-pull type output circuit;
>
> a bus to which the plurality of electronic circuits are connected; and
>
> a termination device having a first non-linear element, and a second non-linear element,
>
> the first non-linear element being connected between a termination voltage line and said bus in a forward direction,
>
> the second non-linear element being connected, in the forward direction, between the bus and a voltage line carrying a voltage lower than a termination voltage supplied via the termination voltage line,
>
> no current flowing in the bus when no signal is transmitted via the bus.

The examiner relies on the following prior art references:

Lloyd 4,808,855 February 28, 1989

Active Terminators For CMOS Drivers, IBM Technical Disclosure Bulletin, Vol. 32, No. 4A, September 1989 (hereinafter "IBM").

THE REJECTION

Claims 40, 41, 43, and 55 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lloyd and IBM. The examiner finds that Lloyd shows a plurality of circuits 14 connected to a bus 10, which is terminated in resistors R1-R4. The examiner finds that "Fig. 4 of Lloyd shows that the electronic circuits (14) have a push-pull type of output circuit (42,44)" (Examiner's Answer, page 4). The examiner concludes that "it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the linear resistor terminators in Lloyd with FETs connected as nonlinear diodes to realize quieting of the bus line as taught by the [IBM] CMOS Drivers reference" (Examiner's Answer, page 5). The examiner states (Examiner's Answer, page 5):

> The p-channel and n-channel FETs in the [IBM] CMOS Drivers reference are connected as diodes (or nonlinear elements) in the same direction and have the same threshold voltages as the diodes of the instant invention. Therefore, the FETs connected as nonlinear

> diodes in the [IBM] CMOS Drivers reference must prevent a current (some current) from flowing in the bus line when no signal is transferred through the bus line in the same manner as the instant invention.

We refer to the Final Rejection (Paper No. 10) and the Examiner's Answer (Paper No. 19) (pages referred to as "EA__") for a statement of the examiner's position and to the Brief (Paper No. 18) (pages referred to as "Br__") for appellants' position.

OPINION

Claims 40 and 55

Claims 40 and 55 seem strangely worded because they recite "no current flowing in the bus when no signal is transmitted via the bus" (emphasis added), whereas appellants describe that a characteristic of the invention is that "no current flows in the termination unit 241 as long as no signal is transmitted via the bus line 240" (emphasis added) (Br5). Appellants argue that "referring to Fig. 26 of the subject application, when no signal is transmitted via the bus line, no current flows along a path including V_{CCQ}, diode 242, diode 213 [sic, 243] and ground in this order" (Br10), which refers to current through the termination unit rather than the bus. The specification describes that "it is possible to

reduce power consumption because no current flows in the termination unit 241 as long as no signal is transmitted via the bus line 240" (page 49). Thus, we wonder whether appellants meant to claim that no current flows in the termination device (instead of in the bus) when no signal is transmitted via the bus. We take the claims as we find them.

Lloyd discloses an improvement in a wire-OR bus. "These transmission lines normally operate between high- and low-voltage states, representing digital ones and zeros. The bus wires are normally biased to reside at their high-voltage states. They are selectively pulled down to their low-voltage states by bus-driver circuits in each coupled element." (Col. 1, lines 22-28.) "The expression wire-OR bus conveys the concept that each wire serves as an OR-gate by changing its state in response to any one of the bus drivers." (Col. 1, lines 32-35.) The resistors R1 to R4 in figure 1 of Lloyd bias the bus to a high-voltage level (col. 4, lines 1-11). "The bus wire is pulled down to the low voltage level whenever one of the bus driver circuits (22) in a system-circuit element (14) connects it to ground." (Col. 4, lines 11-14.) The bus driver 22 has a large transistor which

connects the bus wire to ground when switched on (col. 4, lines 29-35) and an associated precharge circuit 16 which dumps a prescribed amount of charge onto the bus at the moment of each expected transition of the bus to precharge the capacitance represented by the bus wire itself and the bus driver transistor (col. 4, lines 36-44). The precharge transistor and the bus driver transistor may be combined in the arrangement shown in figure 4 (col. 5, lines 9-34). Although the circuit arrangement in figure 4 looks like appellants' push-pull output circuit 236,
it does not function as one because the transistors do not operate
in phase opposition to both source current to and sink current from the bus. The precharge transistor 42 only adds a small amount of charge and the driver transistor delivers about 40 times the amount of current (col. 5, lines 18-21). The wire-OR bus is brought to its high state when the active pull-down device releases the bus, not by the use of a pull-up device. Lloyd discloses that a tri-state bus using pull-up and pull-down devices was known in the prior art (col. 1,

line 63 to col. 2, line 17), although the examiner does not rely on this teaching.

IBM indicates the use of "CMOS-driven transmission lines" (page 393). It is known that CMOS drivers are of the push-pull type. Also, as shown in IBM figure 4, "at the extremes of the operating region, only one of the two transistors is conducting and it is in the square law region" (page 395). Since only one termination transistor is active to source or sink current, the driver must be a push-pull type that sources or sinks current for the high and low logic states. Appellants do not contest that push-pull output bus driver circuits having resistor terminations were well known and, indeed, this is admitted to be prior art in appellants' figure 3. IBM discloses a terminal device comprising diode-connected PMOS and NMOS transistors, i.e., "a simple CMOS inverter wired short circuit common drain to common gate" (page 394), which form a "termination device," as recited in claims 40, 41, and 55. The PMOS transistor is a "first non-linear element being connected between a termination voltage line and said bus in a forward direction," as recited in claims 40 and 41, and has a "rise characteristic" and is a

"first non-linear element being connected, in a forward direction, between a bus and a termination voltage line via which a termination voltage is supplied," as recited in claim 55. The NMOS transistor is a "second non-linear element being connected, in the forward direction, between the bus and a voltage line carrying a voltage lower than a termination voltage supplied via the termination voltage line," as recited in claims 40 and 41, and has a "rise characteristic" and is a "second non-linear element being connected, in the forward direction, between the bus and a voltage line via which a voltage lower than the termination voltage is supplied," as recited in claim 55.

The argued difference between the subject matter of claims 40 and 55 and IBM is the limitation of "no current flowing in the bus when no signal is transmitted via the bus." As we have discussed, appellants may have intended to recite that no current flows in the termination device, instead of in the bus. However, the claims in their present form do not define over Lloyd and IBM. When no signal is transmitted via a bus driven by a push-pull circuit, i.e., when both the pull-up device and the pull-down device are OFF (open

circuited), there is, by definition, no current flowing in the bus since there is no current path between the bus and the supply voltage or between the bus and ground. This is also true of the admitted prior art of figure 3; when transistors 13 and 14 are OFF, there is no current flowing in the bus. Appellants have not shown that current flows in the bus of IBM when there is no signal. Therefore, the rejection of claims 40 and 55 is sustained.

Claims 41 and 43

Claim 41 recites that "a sum of forward direction threshold voltages of the first and second non-linear elements are greater than a difference between the termination voltage and the voltage carried via the voltage line and lower than the termination voltage." Appellants argue (Br10):

> It can be seen from Fig. 3 of the IBM TDB reference that a current flows from the p-channel transistor to the n-channel transistor even when no signal is transmitted via the transfer line. The graph of Fig. 3 shows a current flows from the p-channel transistor to the n-channel transistor even when the voltage described in the horizontal line of the graph is zero.

We do not agree with this reasoning. Figure 3 is a graph of current in the PMOS or NMOS device versus the voltage at the

bus terminal Z and corresponds to appellants' figures 27 and 29. Figure 3 is not meaningful when there is no signal on the bus Z because no signal represents a high impedance condition at Z, not zero volts at Z as argued. In any case, claim 41 says nothing about there being no signal on the bus. Therefore, we find appellants' arguments unpersuasive.

Nevertheless, we find that the claim limitation at issue is not taught by IBM. The threshold voltage of the NMOS device is the voltage between 0 and the point where the upper curve departs upward from the horizontal axis. The threshold voltage of the PMOS device is the voltage between the point labeled Vdd (where the bus voltage at Z equals Vdd) and the point where the lower curve departs downward from the horizontal axis. The difference between the termination voltage Vdd and the lower voltage line (ground) is the voltage between 0 and Vdd. By inspection, the sum of the threshold voltages is not greater than the difference between the termination voltage and ground; the curves would have to overlap along the horizontal axis for this to be true as shown in appellants' figure 27. While it would have been possible to operate the circuit in IBM to meet this condition by

choosing a lower value for Vdd, no motivation has been set forth for making this modification. Accordingly, we conclude that the examiner has failed to establish a prima facie case of obviousness as to claims 41 and 43. The rejection of claims 41 and 43 is reversed.

CONCLUSION

The rejection of claims 40 and 55 is sustained.

The rejection of claims 41 and 43 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS Administrative Patent Judge	)
JOHN C. MARTIN Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LEE E. BARRETT Administrative Patent Judge	)

ARMSTRONG, WESTERMAN HATTORI
McLELAND & NAUGHTON
Suite 1000, 1725 K Street, N.W.
Washington, DC 20006